AMENDMENTS TO THE CLAIMS

Claims 1-30 (Cancelled)

31. (Previously Presented) A processor comprising:

a virtual state mechanism to form a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the virtual state mechanism including

the virtual state reload multiplexer to receive the actual active thread state of the thread; and

the virtual thread state structure coupled with the virtual state reload multiplexer, the virtual thread state structure having a virtual thread state register to generate and store a virtual active thread state based on the actual active thread state, wherein the virtual thread state structure is further to forward the actual active thread state to the state update logic, and the virtual thread state structure to continuously reload the virtual active thread state within the critical update loop until another actual active thread is detected.

32. (Cancelled)

33. (Cancelled)

34. (Previously Presented) The processor of claim 31, wherein the virtual state mechanism is further to form the critical update loop to implement a single cycle

critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

35. (Previously Presented) The processor of claim 34, wherein the processor includes the multi-threaded processor having the plurality of threads.

36. (Previously Presented) A system comprising:

a processor including a multi-threaded processor having a plurality of threads, the processor coupled with a storage medium via a bus, the processor having

a virtual state mechanism to form a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of the plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure;

the virtual state mechanism including

the virtual state reload multiplexer to receive the actual active thread state of the thread; and

the virtual thread state structure coupled with the virtual state reload multiplexer, the virtual thread state structure having a virtual thread state register to generate and store a virtual active thread state based on the actual active thread state, wherein the virtual thread state structure is further to forward the actual thread state to the state update logic, and the virtual thread state structure to continuously reload the virtual active thread state within the critical update loop until another actual active thread is detected.

37. (Cancelled)

38. (Cancelled)

39. (Previously Presented) The system of claim 36, wherein the virtual state mechanism is further to form the critical update loop to implement a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

40. (Previously Presented) A method comprising:

forming, via a virtual state mechanism at a processor, a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the processor including a multi-threaded processor having the plurality of threads, wherein forming includes

receiving, via the virtual state reload multiplexer, the actual active thread state of the thread; and

generating, via a virtual thread state register of the virtual thread state structure coupled with the virtual state reload multiplexer, a virtual active thread state based on the actual active thread state, the virtual active thread state being stored at the virtual thread state register,

forwarding, via the virtual state structure, the actual active thread state to the state update logic; and

continuously reloading, via the virtual thread state structure, the virtual active thread state within the critical update loop until another actual active thread is detected.

41. (Cancelled)

42. (Cancelled)

43. (Previously Presented) The method of claim 40, wherein forming the critical update loop includes implementing a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

44. (Currently Amended) A machine-readable storage medium comprising instructions that when executed, cause a machine to:

form, via a virtual state mechanism at a processor, a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the processor including a multi-threaded processor having the plurality of threads, wherein forming ~~includes~~ causes the machine to:

receive, via the virtual state reload multiplexer, the actual active thread state of the thread; and

generate, via a virtual thread state register of the virtual thread state structure coupled with the virtual state reload multiplexer, virtual active thread state based on the actual active thread state, the virtual active thread state being stored at the virtual thread state register;

forward, via the virtual state structure, the actual active thread state to the state update logic; and

continuously reloading, via the virtual thread state structure, the virtual active thread state within the critical update loop until another actual active thread is detected.

45. (Cancelled)

46. (Cancelled)

47. (Previously Presented) The machine-readable storage medium of claim 44, wherein the instructions when executed to form the critical update loop, further cause the machine to implement a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.